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TINKER

FABRICATION OF SENSOR PACKAGES ENABLED BY ADDITIVE MANUFACTURING

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Executive Summary

Processes required for demonstrator fabrication, like pick&place of bare dies, inspection, printing pattern generation followed by gap filling and printing of conductive patterns, as well as printing of 3D waveguides were validated for small series production.

The placement process developed in WP 3 was successfully applied to precisely place dies into an epoxy-filled cavity on the RADAR printed circuit board (PCB), while controlling spillover. The image and topology data generated during and after bonding were used to generate inkjet printing masks.

A temperature cycling between -40°C and +125°C, all together 25 cycles took place. CT imaging and DC characterization is performed before and after the thermal cycling.

Large cracks through the whole cross-section of the waveguide are visible. The images of the computer tomography show various smaller cracks and delamination between the substrate and the waveguide, as well as between the dielectric and the conductive layer.

During the UV-curing the dielectric shrinks significantly, causing a bending of the PCB-substrate and bringing tension into the structure. This tension increases even further during the thermal cycling, leading to cracks and delamination of the waveguide. The cracks in the waveguide destroy the component completely. Some delamination of the sliver ink from the dielectric surface can be detected as well, however the conductivity is not deteriorated substantially.

For the Infineon radar silicon wafer technology B11HFC a sinter-able pad finish was developed. The contact resistance of printed Ag-ink routing line to new chip pad finish was verified on prototype level. The same pad finish was integrated into FOWL-packaging process as a backup solution for die embedding.

For assessment of the Ag ink printing technologies a test design defined by IFAG, BOS and PRO was printed on boards with embedded DC radar dies. Inkjet printed and NIL printed demonstrator samples were processed and shipped to IFAT for electrical testing. With optimized imprint material DC-test design samples could be produced reaching the required line/space-resolution with a 125µm-pitch and low DC-line resistance values. Reducing linewidth tolerances and further improvement of the imprint material require further process development.

NIL ink printing technology was able to achieve the required line-space-pitch of 125µm. The linewidth tolerance was very good. Some NIL printed cavities showed incomplete fill, some areas showed ink overflow. Samples showed acceptable DC-line resistance values. NIL-printing process development is still in an early stage with potential for large improvements.

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Introduction

The vision of TINKER is to provide a new cost- and resource efficient pathway for RADAR and LIDAR sensor package fabrication with high throughput up to 250units/min, improved automation by 20%, improved accuracy by 50% and reliability by a factor of 100 to the European automotive and microelectronic industry via additive manufacturing and inline feedback control mechanisms. Autonomous driving and self-driving cars represent one prominent example for the use of microelectronics and sensor, most importantly RADAR and LIDAR sensors. Their respective markets have a big potential, e.g. it is estimated that the market size of LIDAR in automotive will double itself in the next two years (within 2020 to 2022).

Figure 1: TINKER overview

The public awareness and the industrial need for further miniaturization of such sensor packages is the main driver of ongoing efforts in the automotive sector to be able to integrate such devices into the car body like in the bumpers and head lamps instead of attaching them (e.g. on top of the car in case of LIDAR device). Safety (for the driver and others) is the most important key aspect of the automotive sector. Therefore, high-value and high performance RADAR and LIDAR systems are required for advanced driver-assistance systems (ADAS) as well as robotic cars. Current bottlenecks are the relatively large size of such sensor devices, their weight and power consumption. Since these factors are highly limited within cars, further miniaturization and improving functionality and efficient use of resources is highly demanded.

Description of deliverable

This deliverable is summary of RADAR sensor package demonstrator fabrication via TINKER pilot platform. The process have been tested for small series fabrication as well. Up to 6 Radar daisy-chai chips have been assembled in one assembly process. Preparation of the printing files for gap filling and interconnections is scalable up to the size of the build tray platform as well as printing of 3D antennas.

1. Radar Sensor Package – Assembly and Contacting

TINKER project is using for pcb die embedding Infineon's automotive 77GHz radar transceiver RXS8160PL. The silicon die is fabricated in a low-power 130nm BiCMOS inhouse technology called B11HFC. The BEOL-stack has six Cu-layers and one final Al-layer, which is used as pad metal. For process development a daisy chain test vehicle (DC) was used. Here only the last Cu-layer (M6, 5µm) and the 860nm Al- metal layers were used, separated by dielectric layers and passivated by 900nm oxide/nitride-passivation stack.

1.1. Chip description

Infineon has developed in WP5 and 6 a sinter-able pad finish process for its automotive radar SiGe-Wafer technology. For building the demonstrator concept1 DC Si-wafer were processes with 2 metal layers, one Cu-layer and one AlCu-layer. The DC dies had the same size and the same pad frame as the corresponding Infineon RXS radar product. Cu was used to realize the DC bridges on the die, AlCu as pad metal. Below and between the two metal layers dielectric materials were processed and on top a nitride passivation. On top of the AlCu-pads the additional 3 um thick NiPPadAu pad finish was processed. In the field of power electronics, it is typically used as universal pad surface which allows following bonding, soldering and sintering processes. Transferring this process to the B11HFC radar technology was an innovative step. Si wafer thickness was reduced from 725µm to 300µm and after mechanical dicing the diced wafers were shipped on dicing frame to BESI and PRO.

TIG has developed in WP5 the acrylate based dielectric ink which is used for filling up the gaps around the microchip after the pick & place process from BESI. The electrically conductive silver ink used for the inkjet printing of the DC-Layout was developed during WP5 from PVN. Additional information about the inkjet inks are found in the public deliverable D5.4.

For processing the sinter-able chip pad pre-treatment was done om a Triton single-wafer wet-etch tool from Semsysco. Electrochemical plating processes were done on an AP&S e-less plating equipment Vulcanio (see Figure 2).

Figure 2: e-less plating tool Vulcanio; source: AP&S

1.2. Characterization Equipment

A measurement setup was compiled for the characterization of the conductive coating of the waveguide antenna (**Error! Reference source not found.**). On each substrate the WG1 and the WG2 antennas were printed and metalized. The ohmic resistance on both waveguides were measured. A self-adhesive copper foil was placed on both ends of the waveguides, along the whole perimeter *D* of the printed structures. These copper foils were attached to four-point-probes of an LCR-Bridge. Since the measurement results lie in the mΩ range, the lowest possible measurement voltage of 20mV was applied. Also, the lowest possible frequency of 20Hz was selected as measurement frequency, since the ohmic resistance was characterized. The measurement was carried out with a Keysight E4980AL LCR-bridge, with an open-, short-calibration performed prior to the measurements.

1.3. Process of Demonstrator Realization

1.3.1. Sinter-able die pad finish

The new die pad finish for the B11HFC-technology was a NiPPdAu layer stack processed in a sequence of several cleaning and electroless plating steps. These processes were taken from power electronic products and transferred to B11HFC-technology. An electroless-plating process was chosen because it can be processed very uniform on the available AlCu-pads without any additional seed layer or lithography. The uniformity is much better compared to galvanic deposition especially at certain topology steps and no deposition occurs at non-metallic surfaces like the passivation.

Before running an electroless-process precleaning steps are mandatory. They needed to be adjusted to the available B11HFC-metal stack to avoid any passivation under etch or AlCu-pad surface damage. Figure 3 shows the pretreatment scheme for an AlCu-pad surface. After cleaning the pad surface a first zincate deposition was done, then a zincate removal step followed by a second zincate deposition. This flow is important for the speed control of the following Ni-plating step to achieve a uniform NiP-layer over the whole pad and over all pads. Zincate is working as a mediator and reduces the electrochemical potential between Ni and AlCu. The electroless plating process starts with a slow self-limiting immersion process - here the electrons are provided by the AlCu-layer. In the next step the much faster autocatalytic process starts, where the electrons are provided by the reducing agent in the electrolyte while the metal surface is acting as a catalysator, and therefore the process is not self- limited. The NiP-deposition can be described in a simplified way with these two reactions:

After 3000nm NiP-deposition a 300 nm Pd-layer is deposited followed by a very thin Au flash (see Figure 4). The P-content in the NiP-layer is in the range of 7-9 % to achieve an amorphous structure with high sinterability.

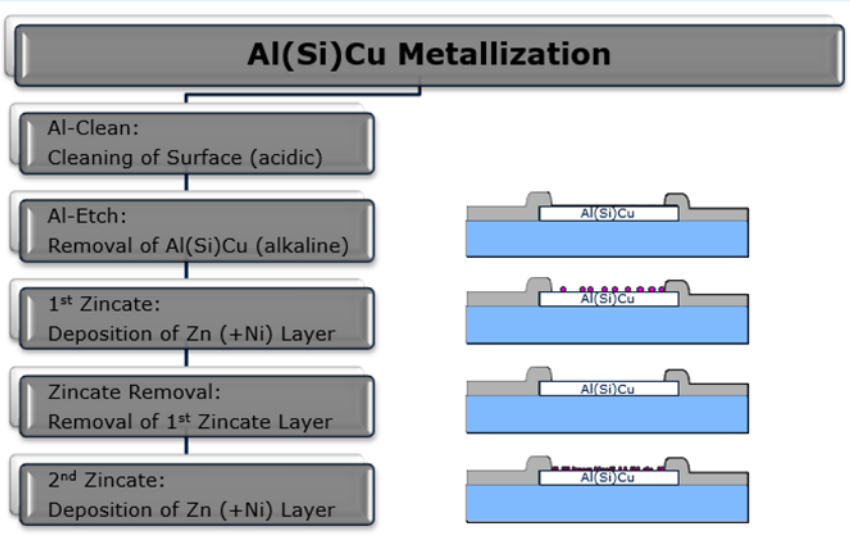

Figure 3: Pre-treatment of AlCu-Pad for following NiPPdAu- stack

Figure 4*:* NiP and Pd electroless plating process steps

1.3.2. Bare die assembly and Evaluation of the P&P process for high-volume production

After the pad finishing process the silicon wafers were tested and singulated on a dicing frame. At this stage the wafers were shipped to BESI for running the die embedding pick and place process. This process was carried out using the best-known method (BKM) developed in WP 3. The assembly process involves dispensing of Loctite QMI536NB automotive grade adhesive, followed by precision die placement, followed by curing. During bonding, an extensive dataset of machine parameters and 2D images were captured.

BESI's contribution to the RADAR demonstrator was to show that the die-in-cavity placement concept (DC Layout printing) is scalable to mass production using commercial pick-and-place hardware. One key development in WP 3 was suitable metrology hardware that allows to capture the right metrics for the TINKER pilot lines. Close alignments between WP 4 (feedback loops and data processing) and WP 3 resulted in a much more streamlined dataset that is efficient to take during bonding but still incurs a significant time penalty for each bond.

During initial process development the focus was on to capture as much data as possible, leading to bond cycles multiple minutes long. The carrier PCBs are also quite small, roughly the size of credit card, with 6 possible bonding positions. BESI's hardware may accommodate much larger substrates up to a width of 200 mm, so that many dies can be placed efficiently. Nevertheless, the basic assessment can be done with the small PCBs as well.

The assembly recipe for the final batch of substrates for the demonstrators was setup to mimic mass production to the best-known methods for the process. The pilot system operates at minimum 150 components per hour (CPH), mostly due to the serialization of tasks that could be done in parallel (e.g. sequential dispensing and placement). BESI's experience with complicated assemblies involving dispensing, placement and inspection is that 300-500 CPH are achievable. Based on the cycle times, a theoretical maximum of 1000 CPH can be estimated, that likely involves a setup that goes beyond the

TINKER pilot line, including dual module machine setup with extra inspection modules to parallelize the inspection and topology measurement steps.

After curing, the 3D topology of the dies in the cavity was measured and forwarded to PROFACTOR (WP4).

1.3.3. Gap filling and printing of the fan-out layout

Based on the 2D and 3D data, images for inkjet gap filling were generated for each chip. The measurements do not cover the whole PCB-area, but each individual chip including its alignment marks. As the precise distances between alignment marks of the chips and the global alignment mark of the PCB are known, it was possible to generate a single printing image (pattern) including all six chips of the PCBs for each layer of the gap filling process.

Thus, the printing process was upscaled as the gap filling process is not required to be performed for each chip individually anymore. For printing, the PCB can be mounted on the substrate plate of the pilot line and the alignment marks will be detected for automated alignment and rotation of the substrate according to the printing pattern. After alignment, the generated patterns are printed layer by layer with dielectric ink on the PCB, filling up the gap between chip and walls of milled PCB-cavity and in a final layer, a dielectric frame in the size of the DC-layout is printed around each chip, finalizing the gap filling process. Each layer is pinned using the implemented UV-lamp and after the last layer, a final UV pass cures the whole structure. The high precision, required for appropriately filling the gaps without covering the contact pads of the daisy chain chip, was reached successfully at the Tinker pilot line.

After gap filling, the DC-layout is printing using conductive ink. As this material is solvent-based, an elevated substrate plate temperature is important for reaching the low line widths without shortcuts. Multiple layers of conductive ink have to be printed in order to get enough material for a proper electric connection, where every layer is dried by the substrate temperature alone. After the final conductive layer, the implemented NIR-lamp heats the structure enough to sinter the nanoparticles to conductive tracks. Apart from high printing precision, the wetting behavior of the conductive ink on the dielectric base is crucial for the successful printing of the thin lines that are required to connect the pads which have very small pitch. Also, this printing process was upscaled, by generating printing patterns for all six chips on each PCB, accounting for the small deviations in location and rotation of the chips within their PCB-cavity (Figure 5).

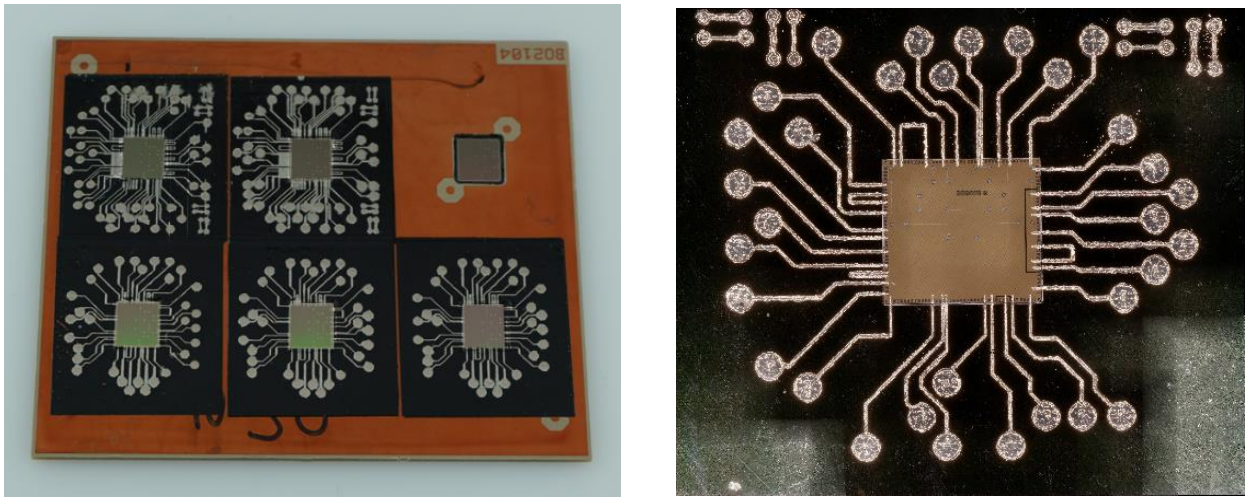

Figure 5: Example of process which was scaled-up to assemble, gap-fill and overprint (dielectric + conductive) 6 bare dies on one PCB carrier (left), detail of one bare die contacted via inkjet printing

1.4. Demonstrator Characterization

A) Inkjet printed sample on glass with black imprinting ink

Silver ink was printed on glass substrate. The optical impression of the relaxed DC-test design was comparable to the previous sample printed on laminate (see Figure 6). No shorts were visible. The linewidth tolerances were comparable, with a linewidth of 70µm and a spacing of 55µm the target pitch of 125µm could be realized. In detail view many line opens were visible at die edges. Large cracks could be seen in contact pad areas. These findings could be confirmed also in the electrical measurement. All measured DC-lines were open, only one dog bone structures had a resistance value of 200 Ohm, much higher than expected.

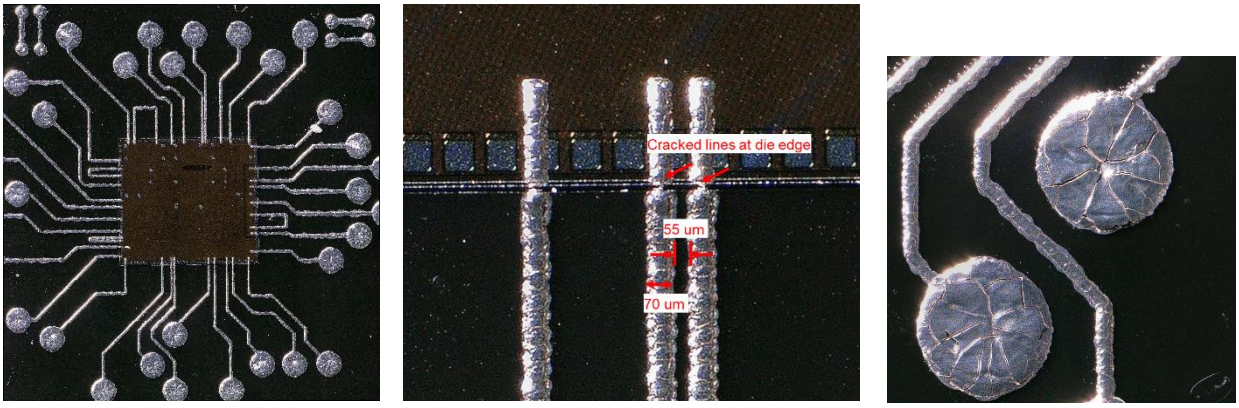

Figure 6: DC Layout on black imprinting material (left), all lines cracked at die edge (centre), large cracks on dog bone structures (right)

B) Inkjet printed sample on laminate using transparent imprinting ink

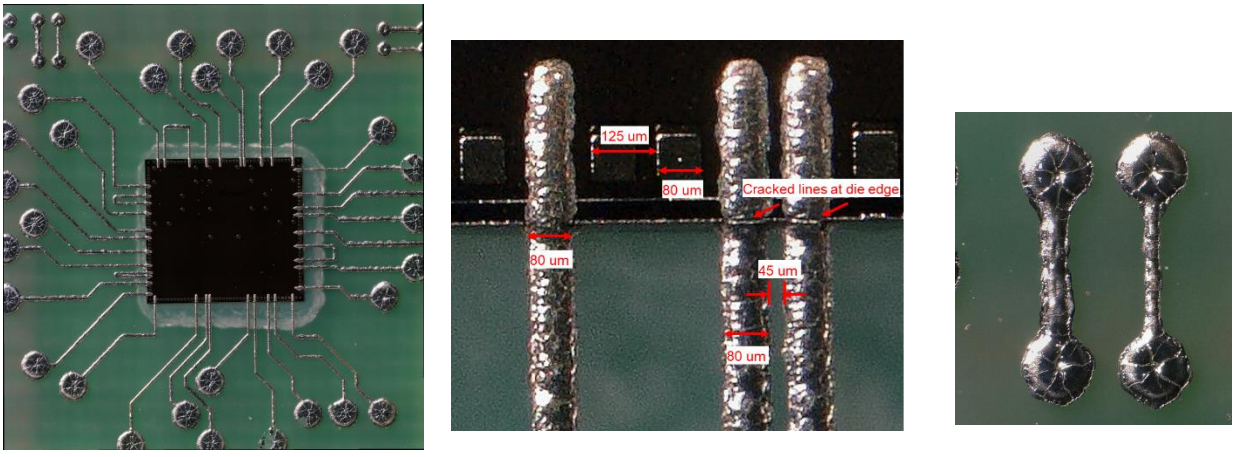

Figure 7: DC Layout on transparent imprinting material (left), some cracks around the microchip could be observed (centre), some cracks on dog bone structures (right)

Silver ink was printed on laminate with 15 stacked layers. The optical impression of the relaxed DC-test design was very good, no shorts were visible. The linewidth tolerances were acceptable and the 125µm line pitch was achieved with 80µm line width and a spacing of 40µm. In detail view (see Figure 7) ink cracks were visible at die edges and at die pads (e.g. dog bone structures). These findings could be confirmed

also in the electrical measurements. Dog bone structures had a line resistance of 2,4 Ohm. Half of the DC connections could be measured with resistances in the range of 14 to 58 Ohm. These values were close to the expected value of 10-20 Ohm. The other DC-bridges were open due to line cracks at the die edge. The transparent imprint material leads to a significant improvement compared to the black imprint material. But further optimization of the imprint material is required.

C) **NIL printed sample with transparent imprinting ink**

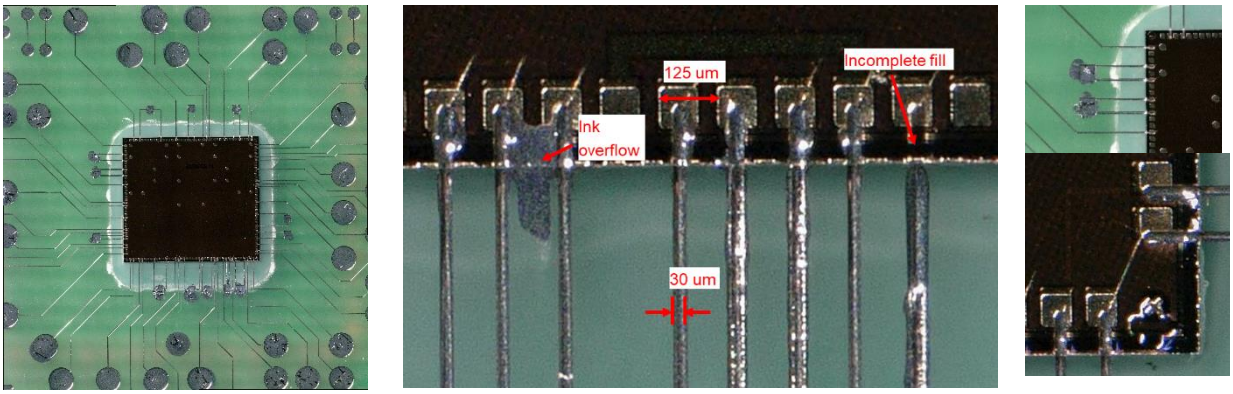

Figure 8: DC Layout on transparent imprinting material (left), ink overflow and incomplete fill at die edge (centre), overflow at printed bridges and misaligned lines (right)

NIL printed samples with target DC-test design showed lines with very fine and uniform linewidth (see Figure 8). Pitch of 125µm could easily be achieved, typical line width was around 30µm. Line to line tolerance was in the range of 50%. At die edge close to the die pads some ink overflows and lines with incomplete fill were found. Ink overflows were also visible at printed bridges due to the additional ink filling squares. On the right side of the die lines were misaligned to the die pads. In the electrical characterization dog bone resistance of 2,1 Ohm and DC bridges in the range of 60-75 Ohm were measured.

Finally, the usage of transparent imprint ink reduced ink crack appearance significantly and lead together with printing improvements to working DC-line structures with low ohmic resistances.

2. Printed Waveguide Antenna

2.1. Fabrication Process

The fabrication process of the metallized waveguide antenna structures is displayed in Figure 9.

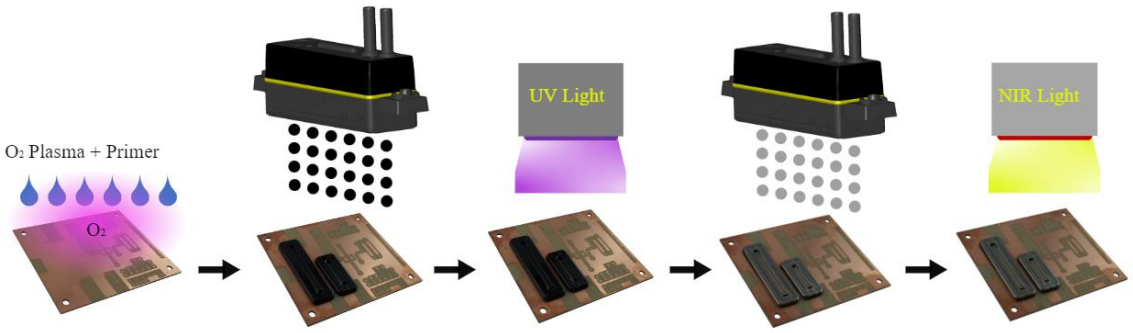

Figure 9: Fabrication process of metallized waveguide antenna structures

Before inkjet printing the copper coated Test-PCBs had to be pretreated with Oxygen Plasma and an adhesion promotor (HMNP12) in order to ensure the adhesion of the black TIG material on the copper PCB. At first the 3D waveguide antenna structure was build up by inkjet printing the black dielectric TIG material on the copper PCB. After every printed layer UV-pinning was done to fix the 3D structure and after the full printing job was done the whole 3D waveguide antenna was fully cured by high intensity UV-Light. Afterwards the 3D waveguide antenna was metallized by overprinting the structure with the conductive silver ink.

The acrylate based dielectric Ink from TIG was used as the 3D material for the waveguide antenna structure. The electrically conductive silver ink from PVN was used for the metallization of the 3D printed waveguide antenna structure.

NIR light was used for drying the printed silver layers as well as for sintering the metallized layer (therefore higher intensity was used). As an alternative to NIR the integrated green laser system can also be used for sintering the metallized layer on the 3D waveguide antenna structure.

In terms of upscaling the TINKER Pilot printer is capable of printing an array of 3x14 antenna structures in one printing job. This can be seen on the image below where multiple 3D antenna structures were printed on copper (Figure 10)

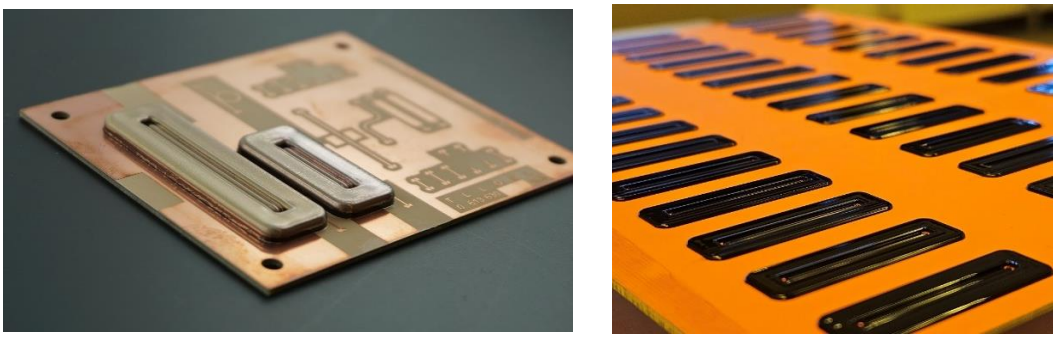

Figure 10: Metallized 3D waveguide antenna structure (left), high throughput production of waveguide antennas without metallization (right)

2.2. Characterization Equipment

The printing process of the 3D waveguide antenna structure inclusively metallization and post processing was performed on the TINKER Pilot Printer. This printer is capable of multimaterial inkjet printing with 4 printheads (Xaar Nitrox) and is equipped with an UV-LED for pinning and curing the dielectric ink, a NIR and a green laser system for post processing of the conductive ink. More information about the TINKER Pilot Printer can be found in the public deliverable Del 5.5.

The waveguides being designed to a carrier frequency of 77GHz, were analysed with a R&S®ZVA90 millimetre converter with samples placed in a on wafer prober (OWP, Figure 11).

Figure 11.: The measurement setup: sample and OWP (on Wafer Probe)

2.3. Demonstrator Characterization

The evaluation timeline of the printed waveguide antennas is shown on Figure 12. Two set of waveguides was analyzed. The high frequency analysis has been carried out on *Waveguide Group 1*. Due to their poor performance, (the results of the RF characterization is described in D7.1) the team decided not to repeat the RF measurements after temperature cycling. In fact, the temperature cycling itself was canceled for the *WG group 1* as well.

The DC properties, such as the sheet and the bulk resistance were characterized for *WG group 2* before and after the thermal cycling. In order to investigate the influence of temperature alternation on crack and delamination of the waveguide structure, CT imaging has been carried out before and after the thermal cycles as well.

All together 25 repetitions have been carried out, on each of them the temperature has changed from -40°C to 125°C back and forth within one hour.

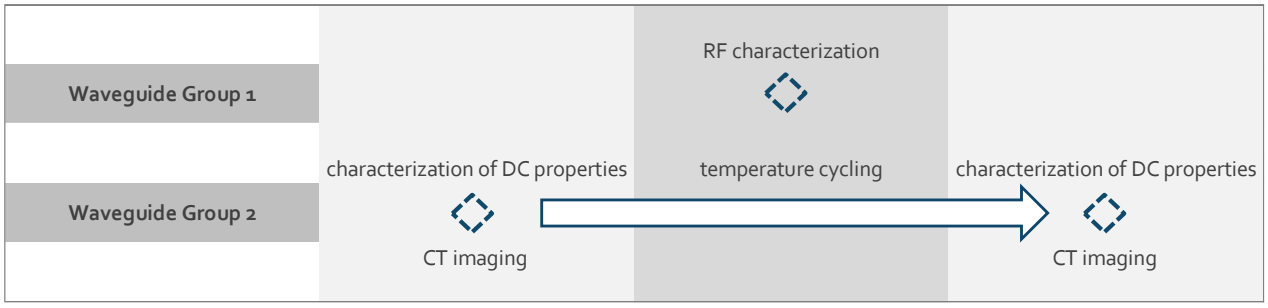

Figure 12.: Timeline of the evaluation of the waveguide samples

As Figure 13 shows after the temperature cycling cracks visible on both waveguides have appeared. There is a crack running through the whole cross-section of WG2 beneath the cover. These cracks are also apparent on the CT image on Figure 14.

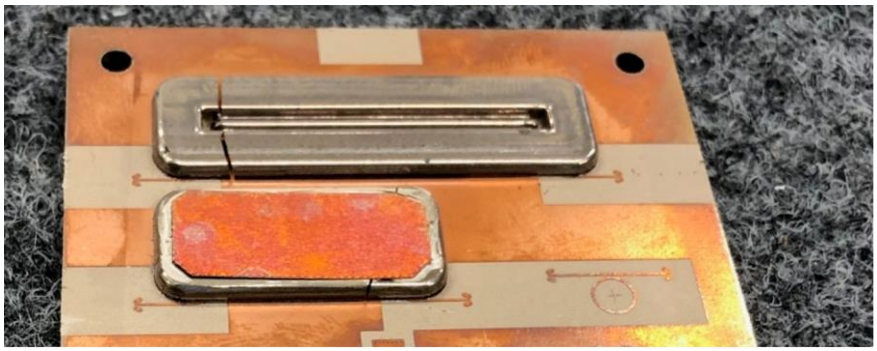

Figure 13.: Cracks are visible on WG1 and on WG2 as well.

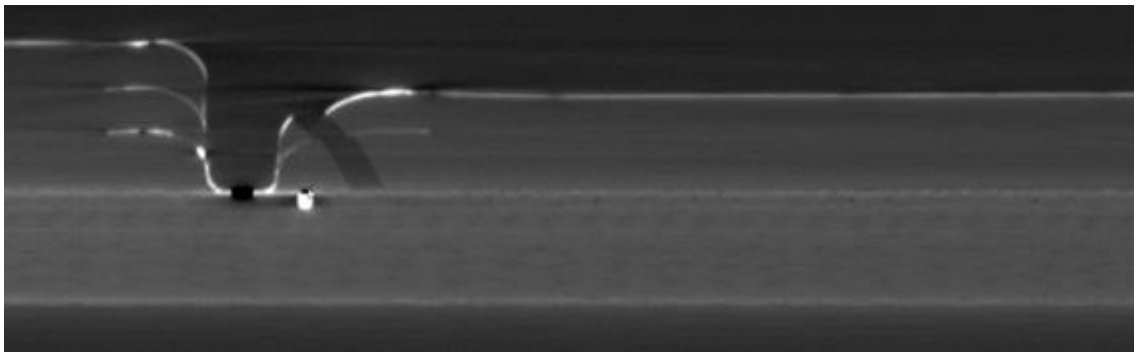

Figure 14.: The crack is visible on the left end of the waveguide channel of WG1

Not only cracks can be observed in the structure, but a delamination between the waveguide and the PCB-substrate as well. Figure 15 shows the cross-section of WG1 after the cycling.

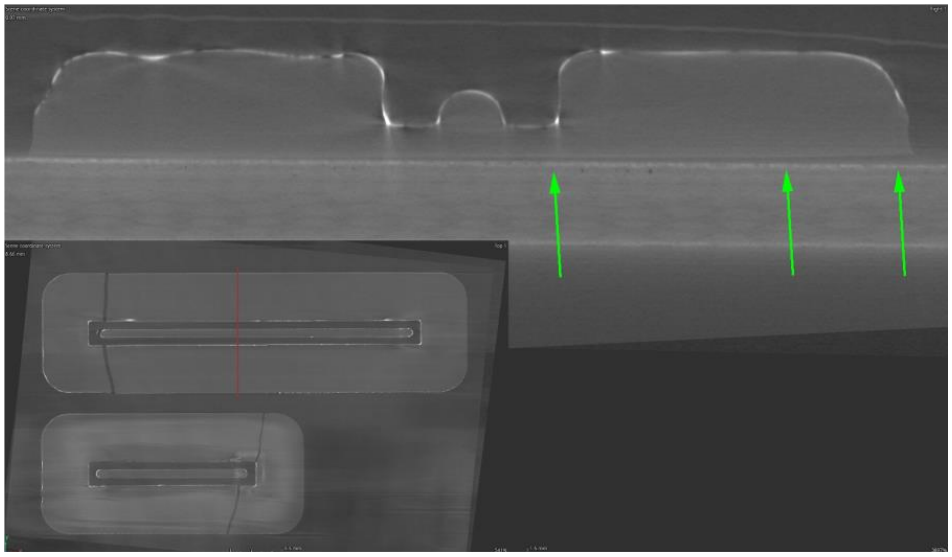

Figure 15.: The CT image of WG1 after the temperature cycling, clear signs of a delamination on the right side of the cross-section

2.3.1. Electrical characterization of conductive layer

Due to the high resolution of the CT-scanner it was not possible to carry out a quantitative analysis of the silver layer. For this reason, sheet resistance measurements were carried out on the specimens before and after the thermal cycling.
At each time an automated Ohmmeter measured the resistance and showed the mean value of the measurements. After measuring all waveguides of all specimens, the whole measurement row was repeated, all together 10 times.
By reading the measurement results, for the first glance it was hard to decide whether the surface conductivity of the specimens has changed. The scatter appearing by comparing the measurement results of the various repetitions was quite large. Some increase in the sheet resistance values after the temperature cycling of specimen 3 (sample 3 was the PCB which has undergone temperature cycling) could be found, however it was still to decide whether these changes are statistically significant. An analysis of variance (ANOVA) was performed to study the statistical characteristics of the measurements. Two groups have been formed for each specimen and for each waveguide. The 0 hypothesis of the analysis was, that these two groups are having an equal population mean (F-test). Generally, the 0 hypothesis is rejected if its probability value (p-value) of the test is above 5%. These p-values are considerably higher for both waveguides of sample 1 and 2. The p-value of the waveguide WG1 of sample 3 is below to the 5%-limit by a great extent, meaning that we have enough evidence to reject the 0 hypothesis. The p-value of waveguide WG2 is 16%, which is far less than the p-values of specimens 1 and 2. However, since this probability exceeds the 5% limit, statistically speaking we do not have enough evidence to reject 0 hypothesis of equal population means. All together it can be stated that in case of the waveguide 2 of the P3 sample there is a statistically significant change in the conductivity of the silver layer, being measured after the temperature cycling.

Table 1.: Results of the ANOVA statistics

	WG1, F	WG1, p	WG2, F	WG2, p
231115_P1	0.001638402	0.969652477	0.081536064	0.789402748
231115_P2	0.00961082	0.926620754	0.000710035	0.980018088
231116_P3	55.11180123	0.001757405	2.928621268	0.162189549

3. Discussion and Results

All together 9 demonstrator PCB have been fabricated for the reliability tests and for the damage analysis. Each demonstrator contained a printed WG1 and WG2 configuration. Copper covers have been glued on the WG2 demonstrator.

14 demonstrator samples of the DC-test design were provided for printed line characterization. 7 samples were inkjet printed and 7 samples were NIL printed, laminate and glass substrates were used and dark and transparent imprint materials.

Capabilities of the individual processes and their suitability for small series fabrication were validated, further testing would be needed to bring the whole process chain to a higher readiness level, but due to delays in the platform realization further test were not performed.

3.1. Waveguide Characterization

A temperature cycling between -40°C and +125°C, all together 25 cycles took place. CT imaging and DC characterization is performed before and after the thermal cycling.

Large cracks through the whole cross-section of the waveguide are visible. The images of the computer tomography show various smaller cracks and delamination between the substrate and the waveguide, as well as between the dielectric and the conductive layer.

During the UV-curing the dielectric shrinks significantly, causing a bending of the PCB-substrate and bringing tension into the structure. This tension increases even further during the thermal cycling, leading to cracks and delamination of the waveguide. The cracks in the waveguide destroy the component completely. Some delamination of the sliver ink from the dielectric surface can be detected as well, however the conductivity is not deteriorated substantially.

3.2. Printed routing line Characterization

Imprint material had a strong impact on crack occurrence. Inkjet printed line/space resolution could achieve the required die pad pitch, but there is only limited potential for further pitch reductions. NIL printed lines have much better line resolutions, but the filling process is still a manual process which needs to be automated and stabilized.

For both printing technologies good line resistances and good line to die pad contact resistances could be achieved. The used NiPPdAu die pad finish fulfilled the sintering requirements.

Characterizations after stress tests could not be performed during the project time frame.