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Executive Summary

The assembly of the LiDAR beam steering prototype, based on the Optical Phase Array (OPA) technology processed on silicon wafers are here reported.

The Tinker fabrication approaches passes through the connexion distribution on the surface of the back side performed by mid process TSV. The main challenge in the Tinker fabrication approaches comes from the fact that TSV development has only been qualified on electronic silicon devices whereas photonic device uses a thick SOI substrate.

The features of the LIDAR prototype will be described in section 2.1; 2.2 section will describe the results of the photonic phase and the OPA beam steering reference tests; 2.3 section will focus on TSV and back side integration; 2.4 the interposer process; 2.5 section will summarize the developments of the flip chip assembly.

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1. Introduction

The vision of TINKER is to provide a new cost- and resource efficient pathway for RADAR and LIDAR sensor package fabrication with high throughput up to 250units/min, improved automation by 20%, improved accuracy by 50% and reliability by a factor of 100 to the European automotive and microelectronic industry via additive manufacturing and inline feedback control mechanisms. Autonomous driving and self-driving cars represent one prominent example for the use of microelectronics and sensor, most importantly RADAR and LIDAR sensors. Their respective markets have a big potential, e.g., it is estimated that the market size of LIDAR in automotive will double itself in the next two years (within 2020 to 2022).

Figure 1: TINKER overview

The public awareness and the industrial need for further miniaturization of such sensor packages is the main driver of ongoing efforts in the automotive sector to be able to integrate such devices into the car body like in the bumpers and head lamps instead of attaching them (e.g., on top of the car in case of LIDAR device). Safety (for the driver and others) is the most important key aspect of the automotive sector. Therefore, high-value and high-performance RADAR and LIDAR systems are required for advanced driver-assistance systems (ADAS) as well as robotic cars. Current bottlenecks are the relatively large size of such sensor devices, their weight and power consumption. Since these factors are highly limited within cars, further miniaturization and improving functionality and efficient use of resources is highly demanded.

1.1. Description of deliverable

Description of EIC assembly LIDAR prototypes via TINKER fabrication approaches.

2. Results and Discussion

2.1. Prototype description

The LiDAR beam steering device is based on the Optical Phase Array (OPA) technology processed on silicon wafers. In this technology, the beam signal is driven from the 1550 nm Laser to the emitting antennas through a silicon photonics device. The photonic part consists in the generation of grating couplers to ensure the coupling with the vertical connection of the fiber array to a horizontal distribution in an optical waveguide made of a Silicon/Silicon oxide interface. Then the waveguide is split in multiple secondary waveguides to create the 256 channels that will consist in the beam feature. In order to ensure the control of the beam signal phase of each channel and thus the beam steering mechanism, each waveguide is locally heated through a specific current passing in a Titanium nitride resistive line named heater that will heat locally the waveguide and modify the signal phase. The waveguides are led to a diffraction feature name antenna that will redirect the light vertically out of the silicon surface plan.

In the description of the project, NIL/Inkjet work in this work package aimed to replace the conventional multiple steps of lithography/etch/stripping of each of the optical features of the silicon technology flow by a single Nanoimprint/inkjet filling process.

However, it became rapidly clear that even if the developments of WP5 were successful in generating the required waveguides, the timeframe to go to a fully integrated process was not compatible with the process of the final demonstrator. As a matter of fact, the waveguides are the first structures to be performed and are followed by 180 process steps. This integration could only be performed in future phase and the presented demonstrator was based on Si/SiO_2 process.

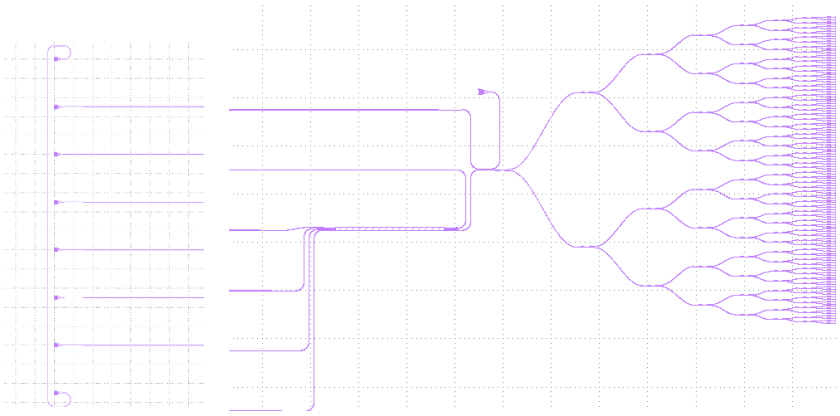
After the optical features are done, the connections from the external channel current control unit pass through Aluminium/copper interconnections. As presented in the definition of the project, this configuration requires a number of cables from the power unit to the PIC that corresponds to the number of channels for both emission and reception so 512 cables for a 256 channels OPA. These external connections need to be located at the edge of the die. In standard semiconductor facilities, the lithography tools specifications limit the die size to around 2.5x2.5 cm which meant for conventional OPAs a wire bonding pitch down to 75 µm which is far below the common wire bonding specifications. The proposition in Tinker LiDAR demonstrator passes through the distribution of the connections from the edge of the top surface to the full surface of the back side one. The connexions between the two faces are ensured by mid process TSV and the redistribution toward the external board will pass through the use of a passive silicon interposer. The connection between the photonic die and the interposer is made using fine pitch lead free solder flip chip technology.

2.2. Photonic results on demonstrator

The process flow used for the realization of the photonic structures of the OPA is a standard process already used for other lots. The dimensions of the grating couplers, the waveguides and the antennas are designed for the selected fiber array and the beam wavelength and adapted to the core/cladding materials index. 8 channels fiber array will be used (6 for signal + 2 for close loop beam control) so 6 wave guides are split to generate the required 256 channels fig 2.2.1 a) and b)

The waveguides and grating couplers consist in etched silicon representing cladding filled by silicon oxide representing the core.

Pictures of the results on demonstrator wafers are shown in figure 2.2.2.



a) grating couplers & waveguides b) splitters

Fig. 2.2.1 : design of the photonic structures of the OPA

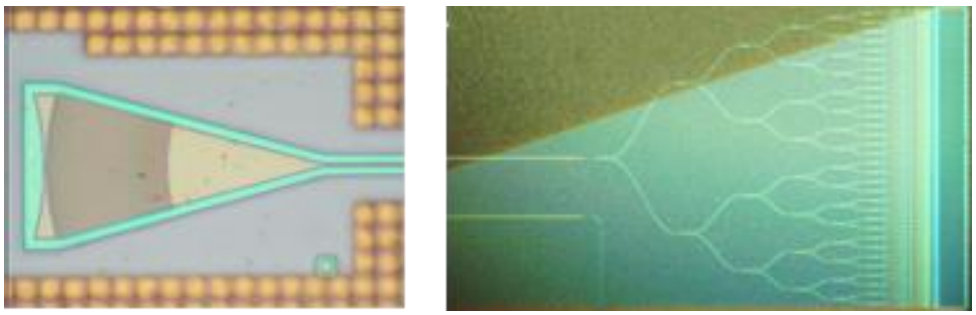


Fig. 2.2.2 : pictures of the photonic structures of the OPA – Grating couplers (left) and splitters (right)

After the photonic phase is performed comes the phase change heaters and the electrical connexions. The design of the heating area is shown on figure 2.2.3. Heaters are consisting in TiN lines designed to provide the required temperature raise by Joule effect. The heaters are connected to the external power supply by W plugs and AlCu metal lines. This process is common and the key parameters to be controlled is the TiN heater dimension and resistivity that have to be adapted to the device specifications. Minimum dimensions are of 400 nm for the waveguide width up to 1µm for the metal lines.

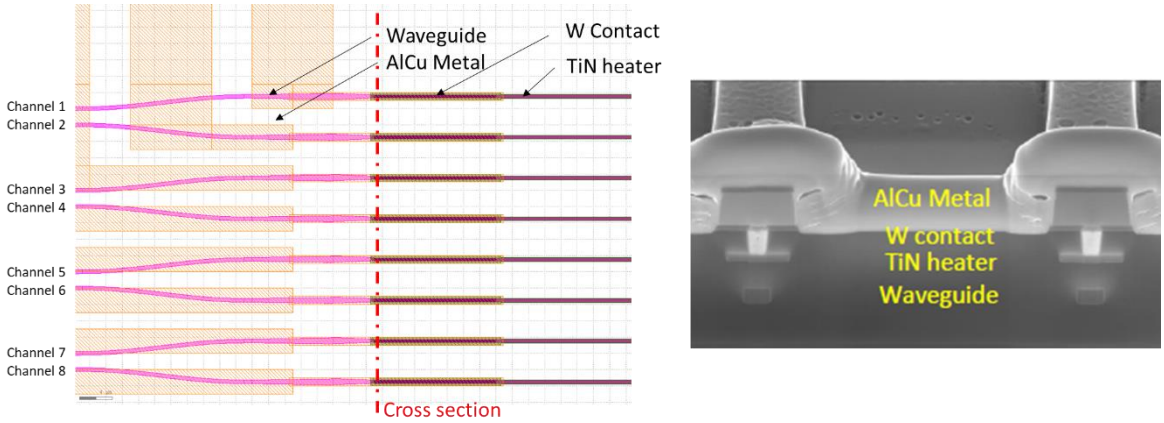


Fig. 2.2.3: description of the beam phase shift area and cross section of the Tinker demonstrator lot

In order to validate the photonic part of the demonstrator lot, a wafer was extracted from the lot and processed using a TSV-less approach as the reference process. Electro-optical tests were then performed to measure the passive functionalities as the beam optical power, the individual channels power consumption … as well as the beam shape and phase shift. Figures 2.2.4 and 2.2.5 summarize the obtained results. On figure 2.2.4, the power

consumption, expected to be 10 mW/channel for a π beam shift is found at 11 mW and is very uniform along the wafer surface. The Optical power variation along the 2π beam steering is also of 22 mW and perfectly distributed.

Figure 2.2.5 shows that all channels are emitting to generate a +/- 20° beam shift and if the absolute intensity is not uniform, this is only due to the fact that the full calibration of the beam wasn't made for this test but will be ono the demonstrator. The beam profile in the scanning direction is at $\Delta\varphi = 0.2°$ for 0.205° in theory . The lot is perfectly in the expected specifications.

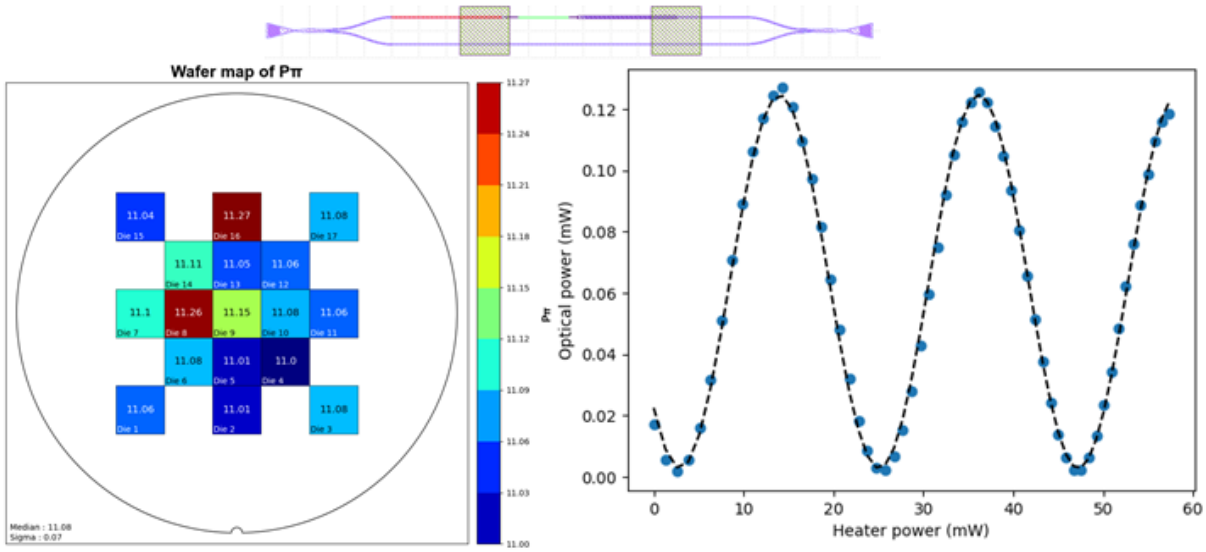


Fig. 2.2.4 : Test of the passive components of the photonic technology: e.g. power consumption and distribution

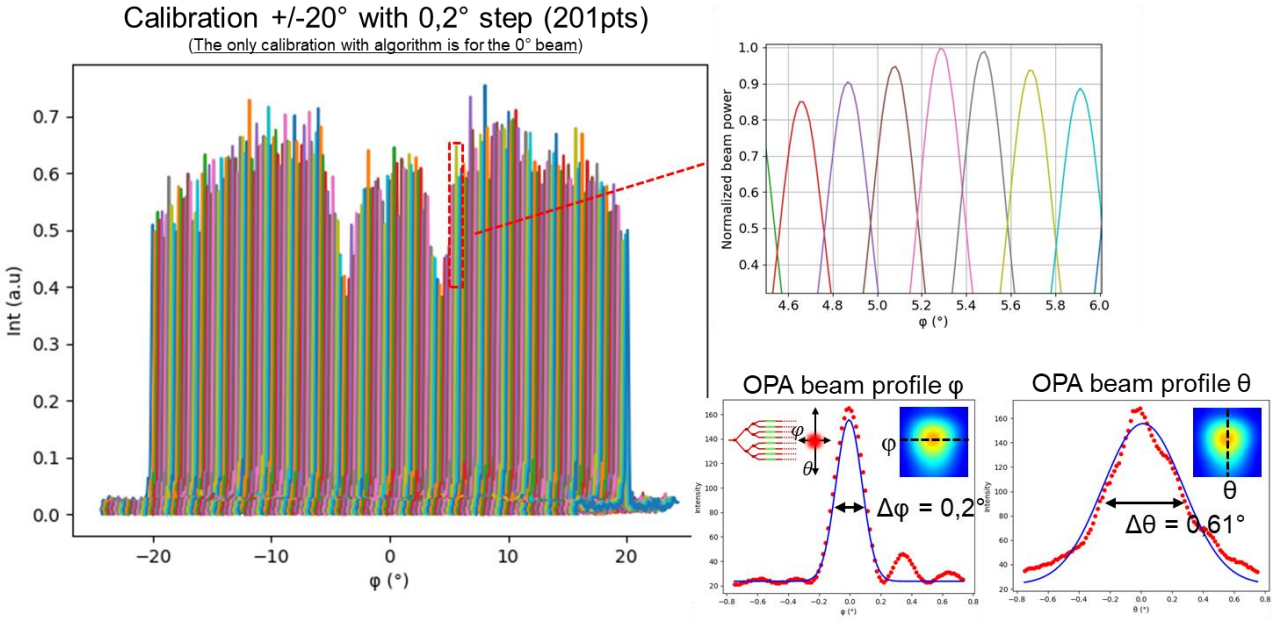


Fig. 2.2.5 : beam profile and shift characterization

After the photonic phase is done, the lot entered in the 3D integration phase

2.3. TSV an µbumps processing

The integration of mid process TSV is a 3D technology already developed for the electronic device 3D integration. It passes through the etch of a blind hole of 10 µm diameter in 100µm of silicon followed by a void free copper filling of this hole and a back side contact recovery to ensure the electrical contact on both faces of the device.

TSV patterning is performed between the W contacts and the AlCu metallization. The main challenge in the Tinker project comes from the fact that TSV development has only been qualified on electronic silicon devices whereas photonic device uses a thick SOI substrate. The presence of the thick SiO2 layer on top of the Si generates a significant undercut when performing the silicon etch as shown on figure 2.3.1. This undercut is critical for the metallization step where a conductive layer made of a Titanium Nitride and Copper stack deposited by iPVD must be continuous in the structure to ensure the electrical distribution inside the TSV during copper electroplating. The undercut led initially to a discontinuous seed layer near the middle of the TSV und thus a lack of copper underneath. Optimization of Titanium nitride and copper seed layer deposition had to be performed leading to a continuous deposition process and a perfect filling of the geometries.

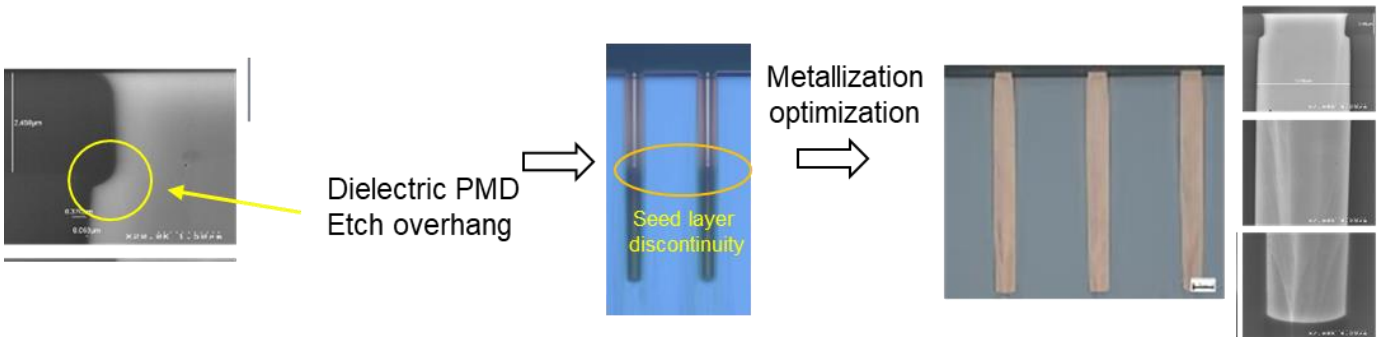


Fig. 2.3.1 : optimization of the mid process TSV copper filling with regard to the photonic substrate configuration

Finally, conventional front side metallization is performed to route the signal toward the heating structures as shown on figure 2.3.2.

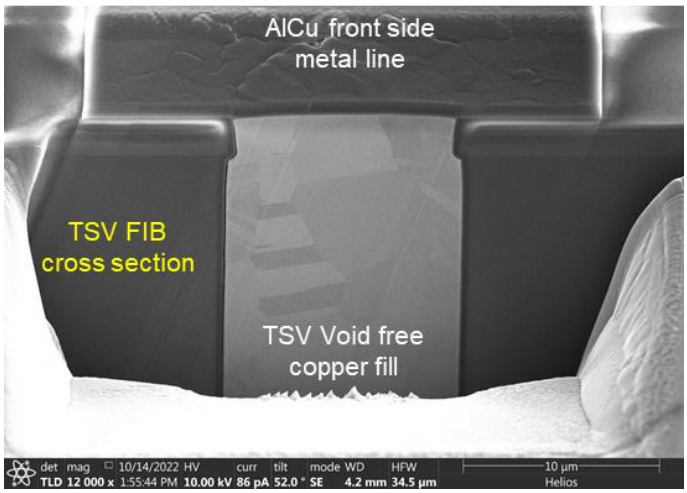


Fig.2.3.2 : Front side metal connection to TSV

The next integration phase consists in bonding the OPA on a carrier using a temporary glue, flip the assembly and grind the OPA back side to reach a thickness of 110µm (staying few µm above the TSV bottom). The key issue here was to validate that the SOI configuration and stress didn't impact the grinding process and that we could reach the target with a Total Thickness Variation (TTV) of the silicon lower than 2µm. Figure 2.3.3 shows this was successfully done. The image made by acoustic microscopy shows also no significant voiding in the glue layer.

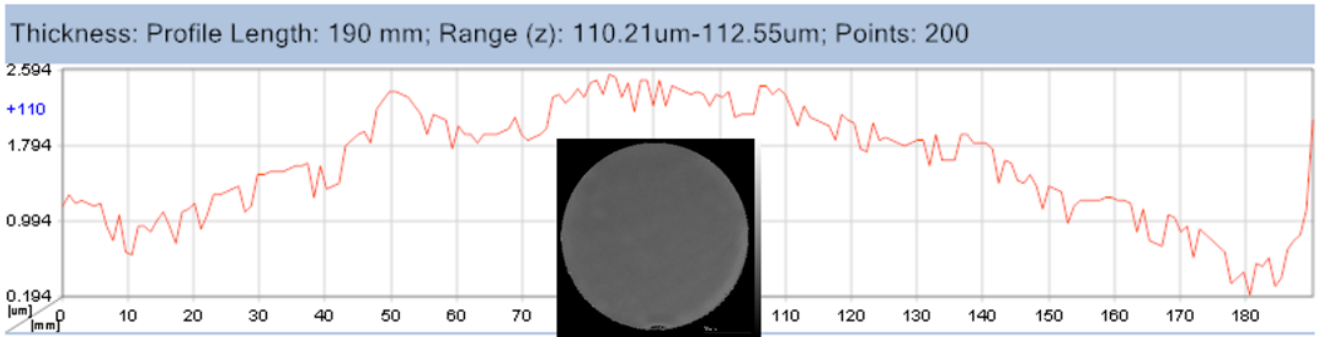


Fig. 2.3.3 : Total Thickness Variation measurement of the Si substrate after grinding to 110 µm

As shown on figure 2.3.4, back side contact with the TSV made using the Copper Nail technology consisting in a SF_6 etch of the silicon down to 5µm more than the TSV bottom followed by TEOS deposition and oxide CMP to reach the TSV copper was performed successfully. However, the processing of the final demonstrator including both photonic and TSV shows a degradation of the contact surface that is related to the behaviour of the Bosch deep RIE etching step on the high resistivity SOI substrate used for photonics. The top surface was perfect but going deep in the silicon, micro-masking starts to be present leading to a so call "grass effect". This is not critical for the Tinker early demonstrator as major part of the dies (see later on electrical tests) are functional and only exhibit a higher dispersion in contact distribution but is clearly a way for improvement to establish a reference integration process.

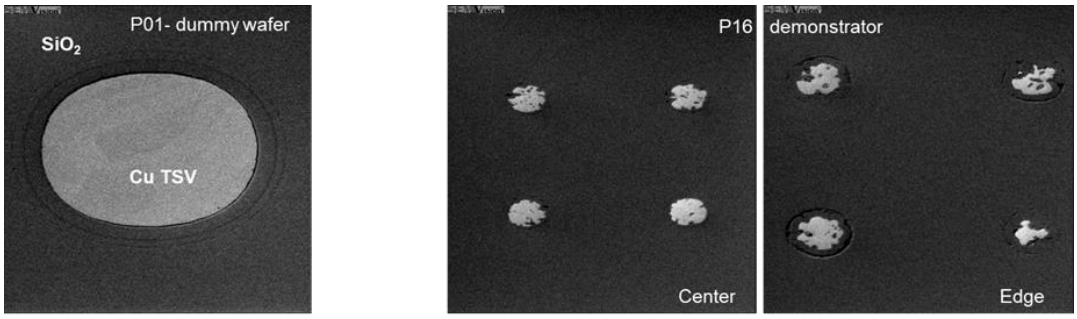


Fig.2.3.4: Back side TSV contact on Si shortloop (left) and thick high Res SOI demonstrator substrates

Finally, the copper RDL routing followed by an organic passivation and the µbumps copper, nickel, Tinsilver electroplated deposition was done with standard processes and gives results in figure 2.3.5 and 2.3.6.

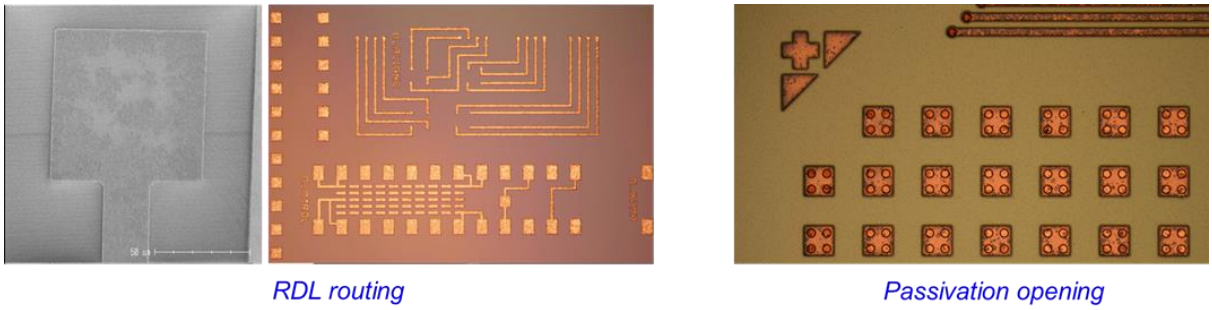


Fig.2.3.5: RDL routing and passivation of the Tinker demonstrator lot

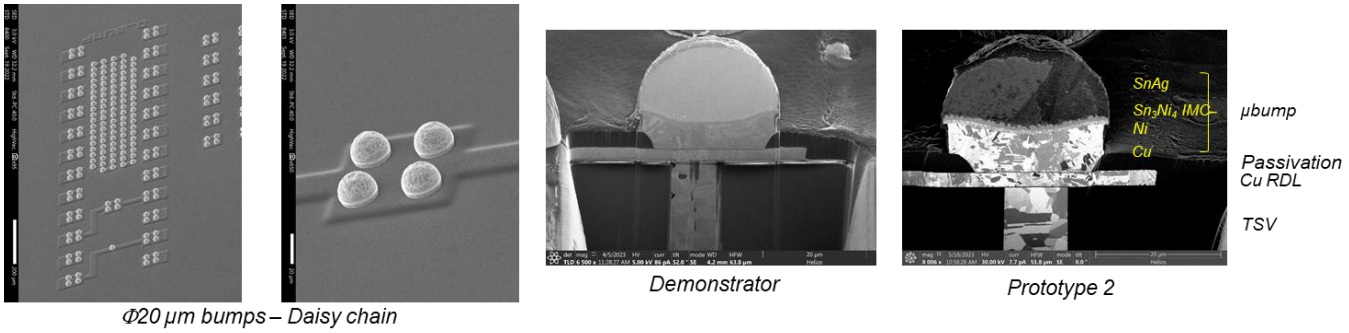


Fig.2.3.6: 20 µm µbumps process on the Tinker demonstrator lot

We can observe again, on the SEM cross section picture, the non-perfect contact between the TSV and the µbump coming from the micro masking effect of the Si etch that will have to be improved in the future.

When bumps are performed, final test of the OPA (the test OPA area) was done to validate the electrical contact between the photonic and the backside of the wafer through the TSV.

The figure 2.3.7 summarizes these tests. On the left part, we can observe the Kelvin TSV contact distribution for both demonstrator and prototype 2 wafers. The yield is 100% for the prototype and few defects are present for the demonstrator wafers (#16,17,20) as well as a larger dispersion, especially for wafer #20. This is not killer but again demonstrates the need for improvement of the deep silicon etch process and the backside contact quality. This can also be observed on the daisy chains on the right part of figure ll. For all chain length from 19 to 96 TSVs, the yield is significantly better for the prototype 2 than the demonstrator for the same reasons. It is emphasized here by the fact that the daisy chain includes only 1 TSV for each contact while the Kelvin and the functional contacts on the demonstrator present 4 parallel contacts which reduces the global dispersion. For the final demonstrator, selection of the best dies will be made for flip chip.

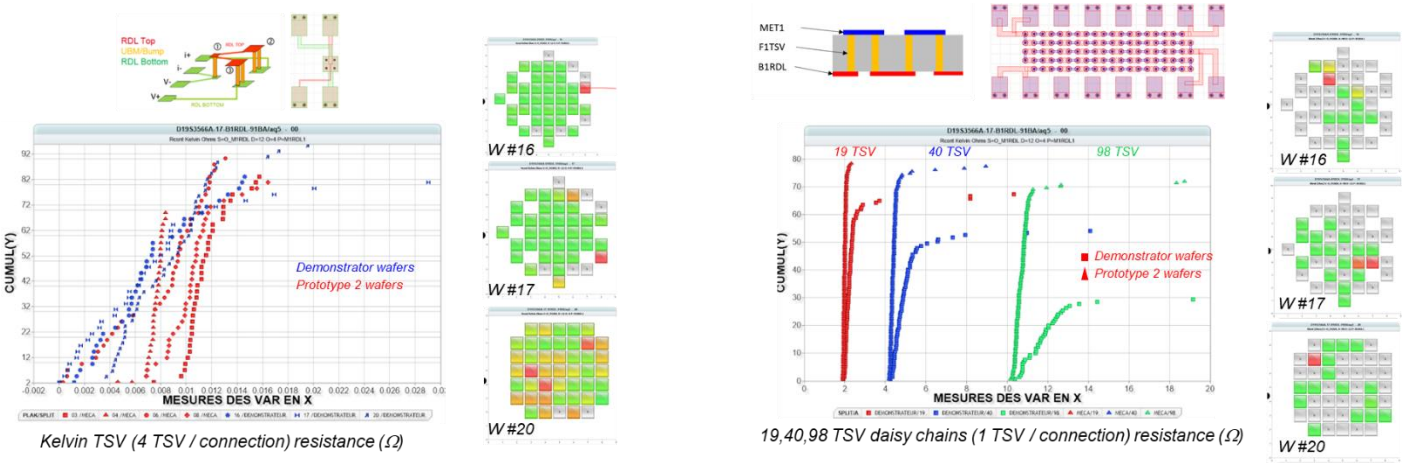


Fig.2.3.7: electrical test of kelvins and daisy chains contacts between front and back side of the OPA

At the stage, the demonstrator lot was ready to be de-bonded and diced to individual dies to enable the flip chip on the interposer. A severe issue on the debonding tool led to a significant delay and required a manual debonding initiation using a blade inserted between the carrier and the OPA. The debonding was good except a bad aspect of the edge of the wafers coming from damages of this blade on the thin silicon of the OPA. However, the dies were clear of defects and no damage was observed during dicing as shown in figure 2.3.8 where we can observe both the damages on the wafer edge and the dicing marks on the frame. It is to be noticed that the tool is being repaired and the normal process doesn't generate these damages, but we needed to go forward the process to be in time for the work package 7 timeframe.

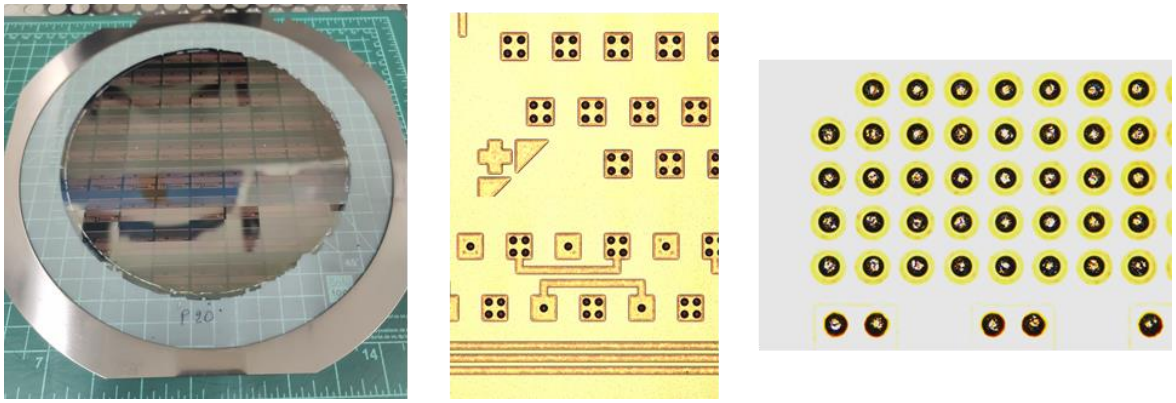


Fig.2.3.8: Demonstrator lot wafer #19 after debonding and dicing

2.4. Interposer process

Considering the interposer process, figure 2.4.1 only summarizes the integration which didn't present difficulties. The metal is performed using a standard lithography / etch of a 440 nm AlCu layer and the contact toward the OPA by flip chip is ensure by a UBM (Under Bump Metallization) made using electroplating of Cu,Ni and Au.

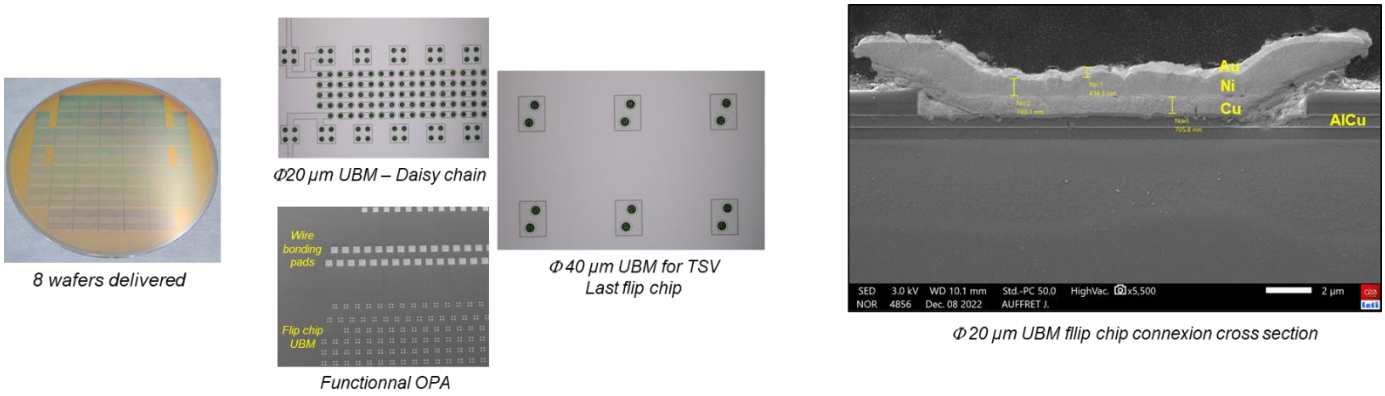


Fig.2.4.1: Interposer wafer processing

2.5. Flip chip process

After dicing, the OPA dies can be flipped chipped on the interposer wafers using die-to-wafer hybridization. The functional OPAs cannot be tested electrically after flip chip so both test and functional OPAs are hybridized to ensure test and functional dies delivery.

Two flip-chip methods can be used to perform the hybridization. The first one is the thermocompression method consisting of simultaneously applying a down force while increasing the temperature up to the SnAg melting point the cooling back to a solid/solid phase. This method has several advantages related to the ability to compensate a significant die deformation as well as an important bump height dispersion often detected when electroplating is not optimal. However, this method requires the temperature raise and decrease for each of the hybridized die which makes it too slow for a mass-volume manufacturing. It is generally chosen for initial work and earl developments.

The second method, the one chosen for manufacturing, is the mass reflow process. In this case, die placement of all the top dies on a wafer is performed at a single temperature then the wafer is heated one time to reach the liquid phase of the solder and cooled to go back to the solidified state. This is much faster than thermocompression but requires flat substrates and a perfect control of the solder surface state that could become critical when solder gets aged as the Tin faces an important and deep oxidation.

The first developments clearly showed a critical issue coming from the warpage of the thin OPA dies. Figure 2.5.1 shows the thermocompression process on the left part and the mass reflow on the right. If thermocompression leads to a contact for both centre and edge of the hybridized dies, stress leaded to some cracks on the edge. Considering mass reflow, the warpage was too high to allow a good bonding and die delamination was observed.

This was confirmed by samples sent to BESI. BESI, as a manufacturing tool supplier, tested a traditional mass reflow approach by placing the dies that were dipped into special fine-pitch flux onto the substrate at room temperature, but they faced the same issues after processing in the reflow oven. This is sown on figure 2.5.2.

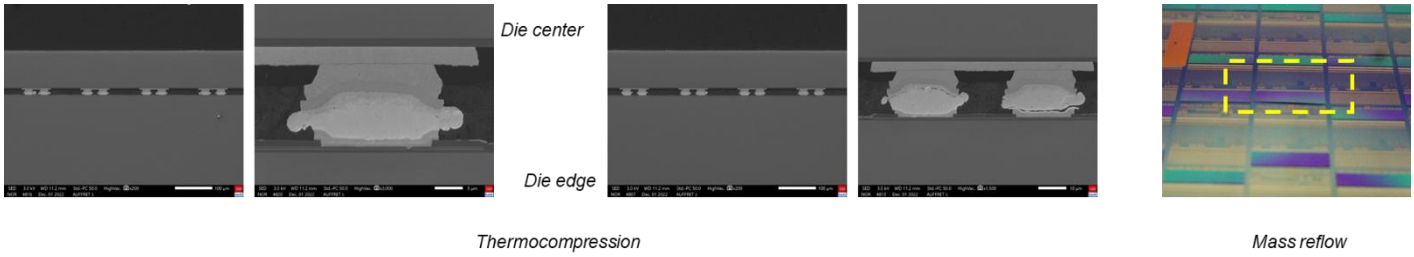


Fig. 2.5.1 : first flip chip trials on prototype 1 dies using thermocompression (left) and mass reflow (right)

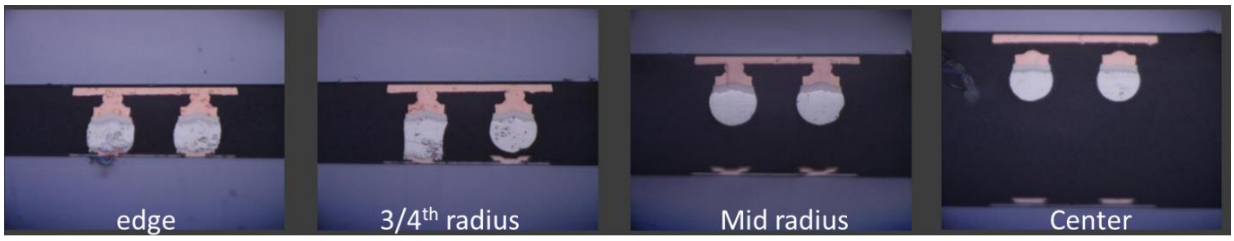


Fig 2.5.2 : Lack of contact on the centre of the die with mass reflow flip chip @BESI due to severe OPA die warping

BESI continued by developing a thermocompression process for a machine based on the 8800 TC*advanced* platform. This approach allows in-situ soldering each OPA while it is being placed by running a tailored thermal profile on a special heated pick tool. This presented some challenges, as the high aspect ratio of the die required a design of the heater that was prone to heat uniformity issues and potentially breakage. An optimized tool design was developed and qualified and is now being used for the TINKER platform.

Using material provided by LETI, BESI optimized the thermocompression bonding process to demonstrate a cycle time of less than 10 seconds at a post-bond lateral placement accuracy of better than 2 µm @ 3 sigma. BESI process experts chose a “safe” set of parameters to conserve precious material during the TINKER process, but see no fundamental obstacles to run it at cycle times of less than 6 seconds. Given the dual-gantry setup of the 8800TCadvanced, it is feasible to bond at a rate of more than 1000 components per hour. This throughput shows the possibility of a highly competitive and cost-effective way of assembling the OPAs for the LIDAR use case in mass production.

Measurement of the thermomechanical behaviour of the thinned OPA using white light interferometry (figure 2.5.3) shows a 200µm bow of the die at room temperature. This decreases when increasing the temperature up to 200°C or more. In the same time, optimization was made on the back side process to reduce the stress by playing on the passivation thickness and add stress compensation layers. These works were implemented on the final demonstrator and less than 100µm bow was achieved which remains a very high value compared to the reference specifications.

However, additional flip chip trials were carried on using this configuration.

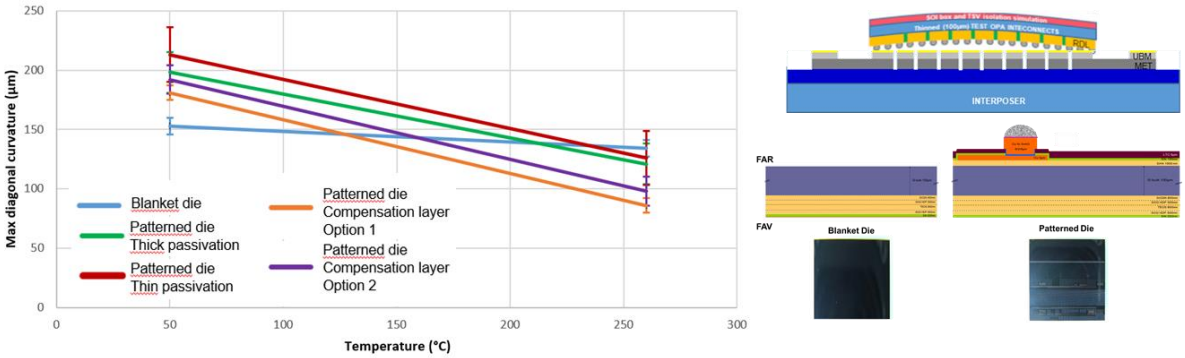


Fig 2.5.3 : Thermomechanical behaviour of thin OPA

Both thermocompression profile optimization and high temperature mass reflow were developed as shown on figure 2.5.4 for the mass reflow results and optimized process point was defined for both solutions and applied on a die to wafer hybridized test wafer.

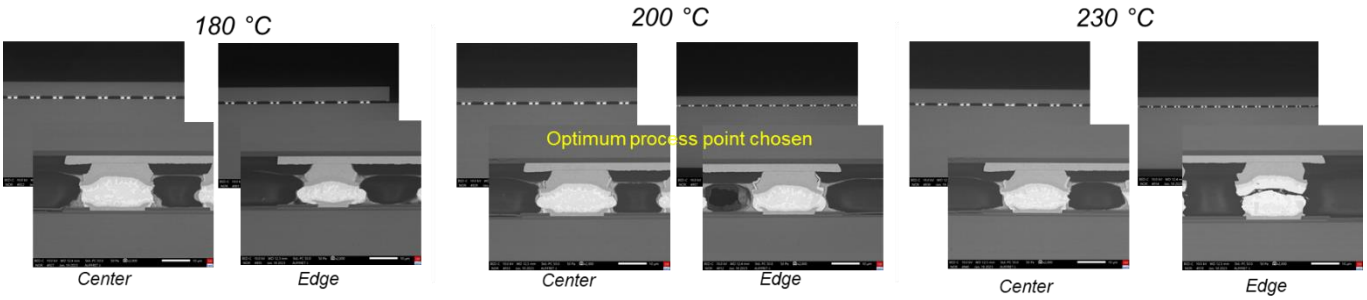


Fig 2.5.4 : mass reflow flip chip optimization

The test wafer was electrically characterized (figure 2.5.5). Both processes give high yield for the kelvin and more important for the wide daisy chain that goes all along the die length and see the full deformation. Mass reflow tends to show sharper distribution compared to thermocompression even if the number of measurements is not sufficient for statistical conclusion.

Both approaches will continue to be applied in parallel for the rest of the project even if the primary choice for the Lidar platform definition will be the mass reflow.

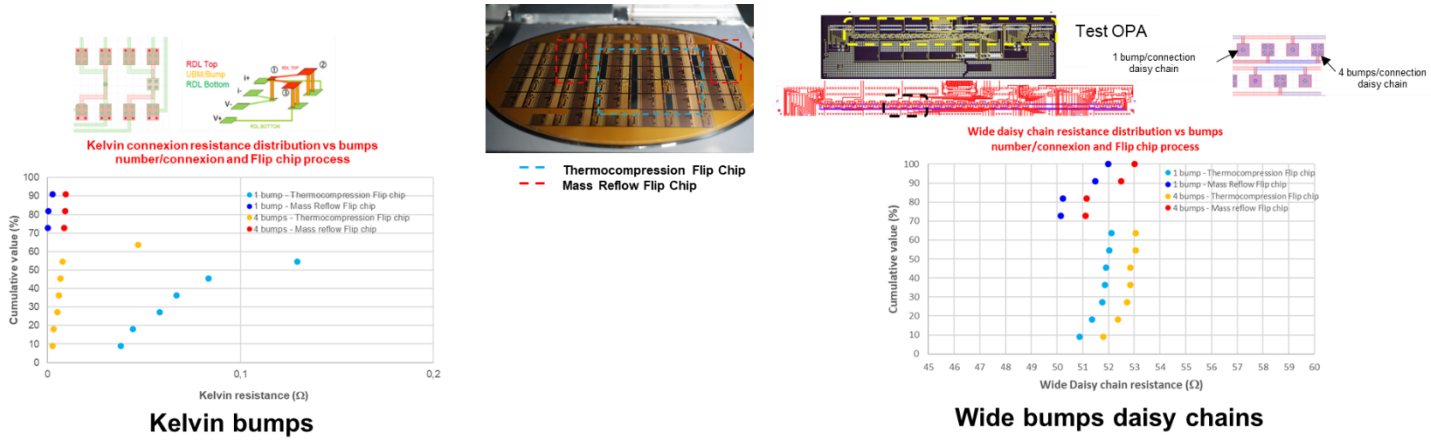


Fig 2.5.5 : mass reflow flip chip optimization

All this work was carried out on the prototypes and is currently being transferred to the demonstrator dies.

Observations on figure 2.5.6 can show the demonstrator before and after flip chip with good results. The complete characterization is under going before the die are sent for electro-optical characterization of the full assembly and further packaging to be delivered to work package 7. We faced delay due to the long down of the debonding equipment as we didn't want to take the high risk of a manual debonding but we finally did it successfully which did not impact the project completion and the delivery of the bonded OPA to the WP7 actors for a full demonstrator completion is expected mid-November.

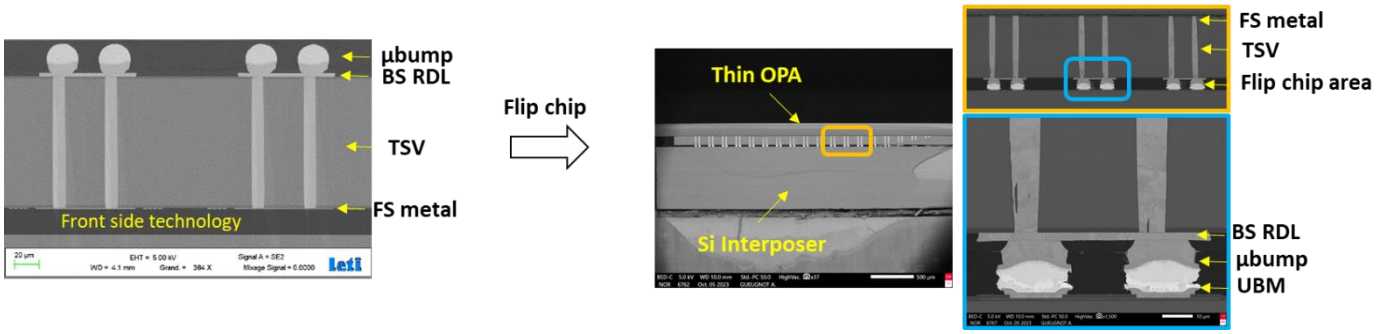


Fig 2.5.6 : OPA cross section with TSV and µbumps before and after Hybridization on the Si interposer

3. Conclusions

The Optical Phase Array feature of the Lidar use case in Tinker project has been successfully integrated with the required advanced features to enable the manufacturing of next generation of Lidars for autonomous driving.

The electrical contacts are moved from the periphery of the top surface to the back side of the photonic device through the integration of the mid process TSV technology. This technology, widely used in electronic devices 3D integration has been adapted to the SOI substrate used for silicon photonic devices and the process is fully compatible with a transfer to mass volume manufacturing or prototyping on CEA LETI silicon platform.

Silicon interposer and fine pitch flip chip technologies were also introduced to reach the requirements of the mobile generation of lidars in terms of footprint and higher integration density while keeping the front side of the photonic device free for the beam input and signal extraction.

Prototyping and mass volume flip chip solutions were successfully evaluated and will be compared in the final integration and packaging in Work Package 7.

4. Outlook

The work described in this deliverable shows the ability to use the CEA LETI silicon platform to build the next generation of Lidars. This passed through the realization of a photonic beam steering device on silicon wafers coupled to TSV, fine pitch flip chip and silicon interposer technologies known for electronic devices integration but not for the integration of a PIC (Photonic Integrated Device) on an EIC (Electronic Integrated Device) using widely known 3D integration technologies and advanced packaging.

In the work package 5, work was done to integrate the photonic technology using additive NIL and Inkjet printing, but we couldn't implement these results in the final demonstrator considering the processing time of the 200 process steps of the OPA integration.

5. Degree of Progress

The demonstrator lot is today fully completed and tested and the die to wafer flip chip technology of the thin and large OPA dies was successfully evaluated.

Additional tests are on-going including final electrical tests after flip chip as well as final electro-optical tests after full integration and should quickly allow the comparison between the 3D and advanced packaging technologies impact on the reference performances of the OPA.

Hybridized dies will be transferred soon for wire bonding and final integration in the demonstrator that will be presented at the LOPEC workshop at the end of the project.

6. Deviation and mitigation strategies

The most critical point was found to be the die deformation of the thinned OPA due to the selected TSV technology. Mid process TSV are limited to 10:1 aspect ratio (depth: diameter) and the diameter is limited to 10 or even 15µm. Considering the SOI substrate and the size of the die, severe deformation is found. A flip chip process was optimized both for thermo-compression or mass reflow, but the process window is expected to be small, and solutions need to be found to increase it.

Stress compensation layers were studied but will be dependent on the integration flow of each future incoming Lidar product so complicated to be implemented on a pilot line.

The second solution is to increase the silicon thickness but as mentioned, mid process TSV are limited in the final aspect ratio.

There is another way to generate the TSV called TSV last integration. This integration, widely used by the OSATs consists in performing the TSV at the end of the silicon flow. The wafer is bonded to a carrier using temporary glue the thinned to the selected thickness (typically in the range of 120 to 300µm).

The TSV patterning is done at this moment and deep silicon etch process has to promote the contact to the front side metal. Considering the depth of the TSV, the complete filing of the TSV is impossible and a copper liner will be done to ensure the contact. More restrictive specifications are put for the aspect ratio of this TSV due to the fact that the temporary glue is limited to a temperature near 200°C which is incompatible with most of the TSV mid process approach. An aspect ratio of 2 to 4:1 is expected which will limit the diameter of the TSV to 50 to 80µm thus reducing the density of the back side connections. However, in the case of the OPA, this was considered as a potential low cost and safer approach.

Evaluation of this solution was then decided and process development of a TSV Last OPA for Tinker is currently on going.

Figure 6.1 shows different results obtained today using this technology and a demonstrator using few OPA wafer with the photonic and front side metallization is under processing. If the demonstrator is completed during project time, we will have the ability to compare the 2 TSV technologies and propose solutions to transfer the technology to low performance and integration density / Low-cost manufacturers (OSATs) or High performance and density / Higher cost ones (IDMs or Foundries) for the future.

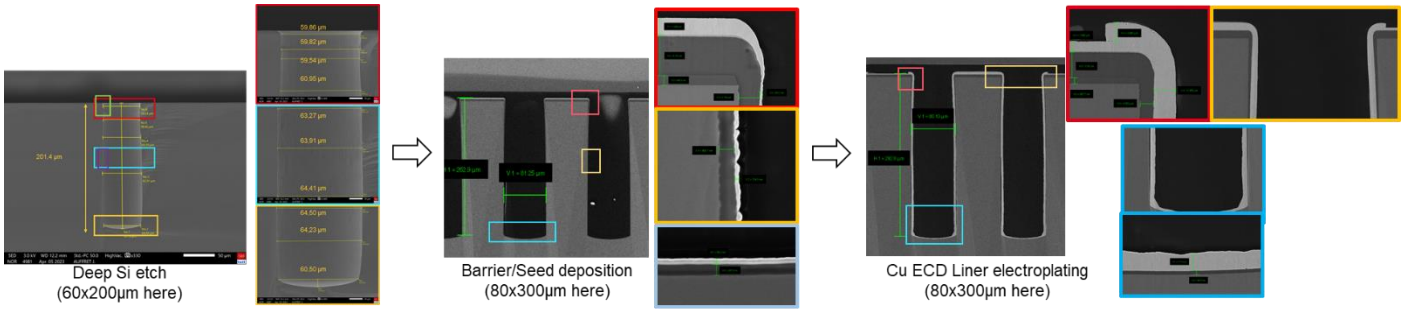


Fig 6.1 : TSV last option development – Deep Si etch (left) and barrier/seed and electroplated copper liner (middle and right) developments